[SPECIFICATION]

[TITLE OF THE INVENTION]

IN-PLANE SWITCHING MODE LIQUID CRYSTAL DISPLAY DEVICE

[BRIEF DESCRIPTION OF THE DRAWINGS]

FIG. 1 illustrates an in-plane switching (IPS) mode liquid crystal display device according to the related art.

FIG. 2 illustrates a plan view showing an in-plane switching (IPS) mode liquid crystal display device according to the first embodiment of the present invention.

FIG. 3(a) illustrates a cross-sectional view taken along line B-B' of FIG. 2.

FIG. 3(b) illustrates a cross-sectional view taken along line C-C' of FIG. 2.

FIG. 3(c) illustrates a cross-sectional view taken along line D-D' of FIG. 2.

FIG. 4 illustrates an optical axis direction in an in-plane switching (IPS) mode LCD device according to the first embodiment of the present invention.

FIG. 5 illustrates a schematic view showing driving of liquid crystal molecules in an in-plane switching mode LCD device according to the present invention.

FIG. 6 illustrates a liquid crystal panel according to the present invention.

FIG. 7 illustrates an in-plane switching mode LCD device according to the present invention.

FIG. 8 illustrates a plan view showing an in-plane switching mode LCD device according to the second embodiment of the present invention.

Description of reference numerals for main parts in the drawings

101, 201: gate line 102, 202: data line

103, 203: common line
105, 205: gate electrode
106, 206: source electrode
107, 207: drain electrode
108, 208: data electrode
109, 209: common electrode
110: first substrate
111: second substrate
112: gate insulating layer
115: active layer
116: n^+ layer
123: alignment layer
125, 225, 325: hole
130: liquid crystal layer
132, 133: liquid crystal molecules
135: polarizing plate
136: analyzing plate
139: liquid crystal panel
140: display part
145: frame
147: backlight housing
148: backlight
149: light-guiding plate
150: gate driving circuit
151: gate pad
154: data driving circuit
155: data pad
157: common pad
160: light-shielding electrode
161: hole
165: external ground circuit
167: static electricity prevention circuit

[DETAILED DESCRIPTION OF THE INVENTION]

[OBJECT OF THE INVENTION]

[FIELD OF THE INVENTION AND DISCUSSION OF THE RELATED ART]

The present invention relates to a liquid crystal display (LCD) device, and more particularly, to an in-plane switching (IPS) mode liquid crystal display device having high resolution and fineness with a decreased manufacturing cost.

Recently, according as the thin film transistor liquid crystal display devices

(TFT-LCDs) have been used as display devices in such applications as portable televisions and notebook computers, it is strongly required to obtain large-sized TFT-LCDs. However, the TFT-LCDs have the problem in that the contrast ratio is changed according to change of viewing angle. In order to solve this problem, twisted nematic LCDs having, for example, optical compensation plates and multi-domains, have been introduced. In these LCDs, however, the color of the image is shifted because the contrast ratio depends on the viewing angle direction.

For a wide viewing angle, the in-plane switching mode LCD is disclosed, for example, in JAPAN DISPLAY 92 P547, Japanese Patent Unexamined Publication No. 7-36058, Japanese Patent Unexamined Publication No. 7-225538, and ASIA DISPLAY 95 P107.

FIG. 1 illustrates an in-plane switching (IPS) mode liquid crystal display device according to the related art. As shown in FIG. 1(a), the in-plane switching mode liquid crystal display device according to the related art includes gate and data lines 1 and 2 formed on a first substrate 10 to define a pixel region, a common line 3 arranged in the pixel region for being in parallel to the gate line 1, a thin film transistor formed at a crossing point of the gate and data lines 1 and 2, and data and common electrodes 8 and 9 formed in the pixel region for being in parallel to the data line 2. As shown in FIG. 1(b), the thin film transistor includes a gate electrode 5 formed on the first substrate 10 for being in contact with the gate line 1, a gate insulating layer 12 deposited on the gate electrode 5, an active layer 15 formed on the gate insulating layer 12, a n^+ layer 16 formed on the active layer 15, and source and drain electrodes 6 and 7 formed on the n^+ layer 16 for being in contact with the data line 2 and the data electrode 8. The common electrode 9 in the pixel region is formed on the first substrate 10 for being in

contact with the common line 3, and the data electrode 8 is formed on the gate insulating layer 12 for being in contact with the drain electrode 7 of the thin film transistor. Then, a passivation layer 20 is formed on the thin film transistor, the data electrode 8 and the gate insulating layer 12, and a first alignment layer 23a is deposited thereon to determine alignment direction.

On the second substrate 11, a black matrix layer 28 is formed to prevent leakage of light through the regions of the thin film transistor, the gate line 1, the data line 2, and the common line 3. Then, a color filter layer 29 and a second alignment layer 23b are formed thereon. Also, a liquid crystal layer 30 is formed between the first and second substrates 10 and 11.

In the aforementioned in-plane switching mode LCD device, an electric field being in parallel to the first and second substrates 10 and 11 is generated between the data and common electrodes 8 and 9 when a voltage is applied from an external driving circuit. Accordingly, liquid crystal molecules aligned in the liquid crystal layer 30 are rotated according the electric field, thereby controlling the amount of light passing through the liquid crystal layer 30.

However, the in-plane switching mode LCD device according to the related art has the following disadvantages.

First, since the black matrix layer 28 is formed to prevent light leakage through the regions of the gate line 1, the data line 2, and the thin film transistor, thereby increasing manufacturing cost. Also, in order to form the black matrix layer 28, it is required to deposit and etch the metal such as Cr or CrOx, or the black resin, so that production yield is lowered.

Second, since the passivation layer 20 is deposited on the data electrode 8, and

the gate insulating layer 12 and the passivation layer 20 are formed on the common electrode 9, the electric field applied to the liquid crystal layer 30 is absorbed into the gate insulating layer 12 and the passivation layer 20, whereby the intensity of electric field applied to the liquid crystal layer 30 is decreased. Thus, driving speed of the liquid crystal molecules is decreased so that the image may be disconnected during driving moving picture.

Third, in case the first and second substrates are not completely bonded to each other during bonding process, the black mask 28 invades the pixel region, thereby causing decrease of aperture ratio. The bonding process has lots of difficulties.

Fourth, in order to avoid the crosstalk according to the electric field generated by the gate and data lines 1 and 2, it is required to obtain a predetermined distance between the actual pixel region and the gate and data lines 1 and 2, thereby lowering the aperture ratio.

[TECHNICAL TASKS TO BE ACHIEVED BY THE INVENTION]

An object of the present invention is to provide an in-plane switching (IPS) mode liquid crystal display (LCD) device, in which a light-shielding electrode is overlapped with a gate electrode and a predetermined portion of a gate line, and the light-shielding electrode is in contact with the gate line, thereby obtaining the IPS mode LCD device having high resolution with decreased manufacturing cost.

Another object of the present invention is to provide an in-plane switching (IPS) mode liquid crystal display (LCD) device, in which a common electrode is overlapped with predetermined portions of gate and data lines, thereby preventing disclination generated by the gate and data lines, simultaneously, obtaining improved aperture ratio.

To achieve these and other advantages and in accordance with the purpose of the present invention, as embodied and broadly described, an in-plane switching (IPS) mode LCD device includes first and second substrates, gate and data lines crossing each other on the first substrate to define a pixel region, a thin film transistor at a crossing point of the gate and data lines, a common line formed in the pixel region for being parallel to the gate line, a data electrode formed in the pixel region for being parallel to the data line, a common electrode formed in parallel to the data electrode, a light-shielding electrode being in contact with the gate line on predetermined portions of the thin film transistor and the gate line, the light-shielding electrode formed as a back gate electrode, simultaneously, preventing light from being incident on the thin film transistor, a first alignment layer formed on an entire surface of the first substrate, a color filter layer formed on the second substrate, a second alignment layer deposited on the color filter layer, and a liquid crystal layer formed between the first and second substrates.

At this time, the thin film transistor includes a gate electrode being in contact with the gate line, a gate insulating layer deposited on the entire surface of the first substrate above the gate electrode, an active layer formed on the gate insulating layer, a n^+ layer formed on the active layer, and source/drain electrodes formed on the n^+ layer.

Also, the data electrode is formed on the gate insulating layer for being in contact with the drain electrode, and the common electrode is formed on a passivation layer for being in contact with the common line through a hole. The data and common electrodes form a storage capacity therebetween, whereby it is possible to apply the dual storage capacity to the LCD device. Also, the light-shielding electrode is simultaneously formed at the same layer as the common electrode so that the light-

shielding electrode is in contact with the gate line through the hole of the passivation layer.

In another aspect, an in-plane switching mode LCD device includes first and second substrates, gate and data lines crossing each other on the first substrate to define a pixel region, a thin film transistor at a crossing point of the gate and data lines, a common line formed in the pixel region for being parallel to the gate line, a data electrode formed in the pixel region for being parallel to the data line, a common electrode formed in parallel to the data electrode for being overlapped with predetermined portions of the gate and data lines so as to prevent disclination from the gate and data lines, a light-shielding electrode formed on the gate electrode of the thin film transistor and a predetermined portion of the gate line for being in contact with the gate line through a hole of a passivation layer, the light-shielding electrode formed as a back gate electrode, simultaneously, preventing light from being irradiated to an active layer of the thin film transistor, a first alignment layer deposited on an entire surface of the first substrate, a color filter layer formed on the second substrate, a second alignment layer deposited on the color filter layer, and a liquid crystal layer formed between the first and second substrates.

[PREFERRED EMBODIMENTS OF THE INVENTION]

Hereinafter, an in-plane switching mode liquid crystal display (IPS-LCD) device according to the present invention will be described with reference to the accompanying drawings.

FIG. 2 illustrates an in-plane switching mode LCD device according to the first embodiment of the present invention. As shown in FIG. 2, a plurality of gate and data

lines 101 and 102 are formed on a substrate, thereby defining a plurality of pixel regions. In the actual LCD device, 'n' gate lines 101 and 'm' data lines 102 are formed on the substrate so as to define '$n \times m$' pixel regions. For reference, one pixel region will be descried in the accompanying drawings. In the pixel region, a common line 103 is formed parallel to the gate line 101, and a thin film transistor is formed at a crossing point of the gate and data lines 101 and 102. Also, data and common electrodes 108 and 109 formed in the pixel region are arranged in parallel to the data line 102. At this time, the data and common electrodes 108 and 109 are formed on the common line 103. The common electrode is in contact with the common line 103 through a hole 125 of a passivation layer. Also, as shown in the drawings, a light-shielding electrode 160 is formed on a gate electrode 105 of the thin film transistor and a predetermined portion of the gate line 101, so that the light-shielding electrode 160 is in contact with the gate line 101 through a hole 161.

FIG. 3(a) illustrates a cross-sectional view taken along line B-B' of FIG. 2. As shown in FIG. 3(a), the thin film transistor includes a gate electrode 105 formed on a first substrate 110, a gate insulating layer 112 deposited on the gate electrode 105, an active layer 115 formed on the gate insulating layer 112, a n^+ layer formed on the active layer 115, and source and drain electrodes 106 and 107 formed on the n^+ layer. At this time, the gate electrode 105 is simultaneously formed with the gate line 101 and the common line 103, which is formed by etching dual metal layers of Mo/Al layers, the Al layer having a thickness of 2000Å and the Mo layer having a thickness of 1000Å deposited by sputtering. Also, the gate insulating layer 112 is formed by depositing an inorganic material such as SiNx on the first substrate 110 at a thickness of 4000Å in a chemical vapor deposition (CVD) method. The active layer 115 and n^+ layer 116 are

respectively formed by etching an amorphous silicon (a-Si) having a thickness of 1700Å and a n^+ a-Si layer having a thickness of 300Å in the CVD method. The data line 102, the source electrode 106, the drain electrode 107 and the data electrode 108 are formed by etching Cr layer having a thickness of 1500Å. As shown in FIG. 2, the gate electrode 105 of the thin film transistor is connected with the gate line 101, the source electrode 106 is connected with the data line 102, and the drain electrode 107 is connected with the data electrode 108.

On the thin film transistor, the gate line 108 and the gate insulating layer 112, the passivation layer 120 of SiNx having a thickness of 2000Å is deposited, and then the common electrode 109 is formed thereon. The common electrode 109 is formed by etching Mo layer having a thickness of 1000Å or ITO/MO layer deposited by sputtering.

Then, the light-shielding electrode 160 is formed in regions of the gate electrode 105 and the gate line 101 on the passivation layer 120. The light-shielding electrode 160 is formed of Mo metal layer having a thickness of 1000Å according to the same process as the common electrode 109. As shown in FIG. 3(b), the light-shielding electrode 160 is electrically connected with the gate line 101 through the hole 161 of the gate insulating layer 112 and the passivation layer 120. Accordingly, when a voltage is applied to the gate electrode 105 from an external driving circuit, the light-shielding electrode 160 forms the same electric potential as the gate electrode 105.

At this time, since the light-shielding electrode 160 is directly formed on the gate electrode 105 beside the passivation layer 120, it is possible to prevent light from a backlight or the external from being incident on the active layer 115 of the thin film

transistor. Accordingly, on turning-off state of the thin film transistor, the active layer 115 is excited so that it prevents leakage current, thereby improving picture quality. Also, the light-shielding electrode 160 is formed directly on the gate electrode 105, whereby it is possible to use the high intensity backlight, thereby improving luminance. Furthermore, the light-shielding electrode 160 is in contact with the gate line 101 through the hole 161, and forms the same electric potential as the gate electrode 105, whereby the light-shielding electrode 160 serves as a back gate electrode. Thus, turning-one current of the thin film transistor is increased, so that switching speed of the thin film transistor is improved. In case of the related art LCD device requiring a specific switching speed, it is possible to decrease the size of thin film transistor, whereby the fineness of the thin film transistor is obtained.

Unlike the related art, because a black mask is not formed on the second substrate 111, it is possible to prevent increase of manufacturing cost and lowering of aperture ratio due to decrease on accuracy of bonding process.

A first alignment layer 123a is deposited on the common electrode 109 and the passivation layer 120. In case of that the alignment layer 123a is formed of polyimide, an alignment direction thereof is determined by mechanical rubbing. In case of the alignment layer is formed of photo-reactive materials such as PVCN (polyvinylcinnamate) or polysiloxane based materials, an alignment direction thereof is determined by irradiation of ultraviolet light. In the light-alignment process, the alignment direction of the alignment layer is determined according to the polarizing state, the polarizing direction and the number of light irradiation. Generally, if the polysiloxane or PVCN based materials are used for the alignment layer, the alignment direction is determined by irradiating the ultraviolet light at one or two times. In the

method of irradiating the light at one time, it is possible to irradiate non-polarized light, polarized light (especially, linearly polarized light), or partially polarized light to be slant on the alignment layer. In the method of irradiating the light at two times, it is possible to irradiate polarized light to be slant on or vertical to the alignment layer at one time, after determining the two alignment directions of degeneracy, the polarized light is irradiated again, whereby the desired alignment direction is selected.

As shown in FIG. 2, a hole 125 is formed in the passivation layer 120, whereby the common electrode 109 is in contact with the common line 103 through the hole 125. FIG. 3(C) illustrates a cross-sectional view taken along line D-D' of FIG. 2, which shows the contact of the common line 103 and the common electrode 109 by the hole 125. As shown in the drawing, the data electrode 108 and the common electrode 109 are respectively connected with metal lines formed on the gate insulating layer 112 and the passivation layer 120. In this case, the metal lines are simultaneously formed of the same metal material as the data electrode 108 and the common electrode 109. Accordingly, the gate insulating layer 112 and the passivation layer 120 are respectively deposited between the common line 103 and the metal line being in contact with the data electrode 108, and between the metal line being in contact with the common electrode 109 and the metal line being in contact with the data electrode 108. That is, as shown in the drawings, a total storage capacity Cst of the present invention is formed of the sum of first and second storage capacities Cst1 and Cst2, the first storage capacity Cst1 between the data electrode 108 and the common electrode 109, and the second storage capacity Cst2 between the common line 103 and the data electrode 108, the total storage capacity Cst of the present invention is greater than that of the related art Cst2. Accordingly, the voltage applied to the liquid crystal layer 130 is stabilized. Also,

even though the storage capacity similar to that of the related art is applied, it is possible to improve the aperture ratio since storage capacity region is decreased. Furthermore, the common electrode 109 is formed on the passivation layer 120, whereby adsorption of electric field by the insulating layer is not generated, thereby applying the electric field having great intensity to the liquid crystal layer 130. Thus, the driving voltage is lowered.

On the second substrate 111, a color filter layer 129 is formed. In the color filter layer 129, one of R, G and B layers are repetitively formed in each pixel region. After depositing the second alignment layer 123b of polyimide or photo-reactive material on the color filter layer 129, the alignment direction is determined by rubbing or light irradiation. Also, liquid crystal is injected between the first and second substrates 110 and 111 in a vacuum state, thereby forming the liquid crystal layer 130.

FIG. 4 illustrates optical axis direction of the LCD device according to the first embodiment of the present invention, and FIG. 5 illustrates driving of liquid crystal molecules. In the drawings, θ_{EL}, θ_R and θ_E respectively indicates the extension direction of the data electrode 108 and the common electrode 109, an alignment direction of the alignment layer, and an electric field direction between the data and common electrodes 108 and 109. As shown in the drawings, the data electrode 108 and the common electrode 109 are formed in parallel to the extension direction of the data line 102 (θ_{EL}=90°). Also, the alignment direction determined in the alignment layer (θ_R) is $0° < \theta_R < 90°$. As shown in FIG. 5, the liquid crystal molecules are aligned according to the alignment direction θ_R. As a voltage is applied to the electrodes, the electric field of θ_E=0° is generated between the data and common electrodes 108 and

109. Thus, the liquid crystal molecules 132 are rotated in the clockwise direction, whereby the liquid crystal molecules 132 are aligned along the electric field direction θ_E. In the drawings, the liquid crystal molecules of spotted line show the liquid crystal molecules when the voltage is not applied, and the liquid crystal molecules of solid line show the liquid crystal molecules when the voltage is applied.

FIG. 6 illustrates a thin film transistor array substrate according to the present invention. As shown in FIG. 6, the respective gate and data lines 101 and 120 crossing each other for defining the pixel region are in contact with the external driving circuit through gate and data pads 151 and 155. Also, the gate line 101 and the data line 102 are in contact with the external ground line 165 through the static electricity prevention circuit 167 formed of the thin film transistor. The static electricity prevention circuit 167 is formed between the gate and data lines 101 and 102. The source and drain electrodes of the static electricity prevention circuit 167 are in contact with the data line 102. Also, the common line 103 is grounded on the external through the common pad 157.

Although not shown, the pad 151, 155, 157 is formed of a plurality of metal layers. At this time, the first metal layer is generally used of Mo/Al layer, and the second metal layer is formed of Cr layer. Also, in case of that the common electrode 109 deposited on the passivation layer 120 is formed of ITO/Mo layer, ITO is deposited on the pad 151, 155, 157, thereby preventing increase of contact resistance generated by oxidation of the metal layer on the pad.

FIG. 7 illustrates the in-plane switching mode LCD device according to the present invention, in which FIG. 7(a) illustrates a plan view, and FIG. 7(b) illustrates a cross-sectional view taken along line E-E' of FIG. 7(a). As shown in FIG. 7(a), a gate

driving circuit 150 and a data driving circuit 154 are arranged inside an external frame 145 of a display part 140, whereby the gate and data driving circuits 150 and 154 are in contact with the gate and data lines 101 and 102 of the display part 140 through gate and data pads 151 and 155.

As shown in FIG. 7(b), a backlight 148 is provided inside a backlight housing 147 on the external frame 145, whereby light is projected on the liquid crystal panel 139 through a light-guiding plate 149. Then, a polarizing plate 135 is formed between the light-guiding plate 149 and the liquid crystal panel 139 so as to linearly polarize the light, and an analyzing plate 136 is formed outside of the liquid crystal panel 139.

FIG. 8 illustrates the second embodiment of the present invention. As shown in the drawing showing the second embodiment of the present invention, the second embodiment of the present invention has the same structure as the first embodiment of the present invention except the shape of a common electrode 209. That is, a thin film transistor is formed at a crossing point of gate and data lines 201 and 202, and a data electrode 208 inside a pixel region is formed at the same layer as the source and drain electrodes 206 and 207 of the thin film transistor. The common electrode 209 formed on a passivation layer 209 is partially overlapped with the gate and data lines 201 and 202, and is electrically connected with a common line 203 through a hole 225. By overlapping, the common electrode 209 prevents an electric field generated by the gate and data lines 201 and 202, whereby preventing the disclination on a screen. Also, the overlapping portion serves as a black mask so that it prevent light leakage on regions of the gate and data lines 201 and 202. Accordingly, it is possible to decrease manufacturing cost and to prevent lowering of aperture ratio by bonding fault of the first and second substrates 110 and 111. In the second embodiment of the present

invention, a light-shielding electrode 260 is formed on a predetermined portion of the gate line 201 and a gate electrode 205, so that the light-shielding electrode 260 serves as back gate electrode, simultaneously, the light-shielding electrode 260 prevents light of the backlight or the external from being incident on an active layer 215. As mentioned above, in case the common electrode 209 is overlapped with the gate line 201 and the data line 202, parasitic capacity of the gate and data lines 201 and 202 is increased, thereby generating signal delay. In this respect, the gate and data lines 201 and 202 are formed of low-resistance material such as Mo layer, Mo/Al/Mo layer, or Cr/Al/Cr layer so as to prevent the signal delay.

[ADVANTAGES OF THE INVENTION]

As mentioned above, the in-plane switching mode LCD device according to the present invention has the following advantages.

Unlike the related art IPS mode LCD device forming the black matrix layer for preventing the light leakage on the thin film transistor, the IPS mode LCD device according to the present invention forms the light-shielding electrode on the gate electrode and the predetermined portion of the gate line, whereby the light-shielding electrode serves as the back gate electrode, simultaneously, prevents the light from being incident on the active layer of the thin film transistor, thereby preventing the current leakage. Thus, it is possible to manufacture the IPS mode LCD device having the improved picture quality and fineness with the decreased manufacturing cost. Also, the common electrode is overlapped with the predetermined portions of the gate and data lines. As compared with the aperture ratio in the related art IPS mode LCD device where the gate and data lines are apart from the actual pixel region so as to

prevent the crosstalk generated by the gate and data lines, the IPS mode LCD device according to the present invention obtains the greater aperture ratio.